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High-Power High-Performance Low-Cost Capacitor Charger Concept and Implementation

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***Abstract*—A 20-kJ/s 10-kV 1-kHz repetition rate capacitor charger design and testing are described. The goal of the development was to combine high performance and versatility with low-cost design and good manufacturability. This goal was met using an energy-dosing converter topology with smart controls adapting the switching frequency in such a way as to ensure zero-current switching for all possible scenarios, keeping maximum duty cycle for high power. The switching is accomplished at a frequency of up to 55 kHz, employing relatively slow insulated-gate bipolar transistors with low conduction losses. High efficiency allows all-air cooled design that fits into a $19'' \times 10'' \times 24''$ rack. Design guidelines are reviewed. Comprehensive PSpice models accounting for numerous parasitic parameters and mimicking controls for the frequency variation were developed and simulation results are presented. Worst-case repeatability analysis has been performed. Both PSpice simulations and analytical tools predicted pulse-to-pulse repeatability of 0.3%; the measured figures are 0.8% and 1% for short- and long-term operations, respectively, at peak charging and repetition rates. Typical current and voltage traces and results of thermal runs are presented.**

***Index Terms*—Capacitor charging, power conditioning, power electronics, pulsed power, pulse-to-pulse repeatability (PPR).**

I. Introduction

CAPACITOR chargers are ubiquitous in industry, science, and healthcare. The list of applications associated with pulsed power is very long and ever expanding; the reader may consult relevant sources [1], [2].

Switch-mode power supplies (PSs) almost universally superseded line-frequency PS in capacitor charging. For charging rates above several kJ/s, soft-switching topologies prevail [3]–[9], at least in commercial products (see, e.g., papers from General Atomics [3] and Lambda [4]). Series-resonant topologies seem to dominate this niche. PSs based on these topologies act as a constant current source, and as such are advantageous in limiting the inrush current and protecting the load. With constant current, the charge voltage grows linearly, and thus the charge power is a linear function of time.

Between numerous applications, a combination of high voltage, high charging rate (tens of kJ/s and higher), high pulse repetition rate (PRR), compactness, high efficiency, and good pulse-to-pulse repeatability (PPR) is most difficult. Putting constraints of low-cost and good manufacturability makes the charger development even more challenging. They restrict use of costly custom-made components, fast switches (e.g., wideband gap devices or stacks of fast MOSFETs), exotic cooling schemes and materials (heat pipes, fluorocarbon low-temperature boiling liquids, polymers with nanofillers), leaving relatively few degrees of freedom, such as choice of proper circuit topology and control strategy to increase the switching frequency with the purpose of shrinking the size and improving PPR.

PPR, denoted further as R, is an important parameter in capacitor charging. It influences the stability of various physical processes ranging from lasing to pulsed microwave and X-ray radiation to plasma chemistry applications.

PPR can be defined as

$$R = \frac{V_{C\max} - V_{C\min}}{V_{C\mathrm{avg}}} \cdot 100\% \tag{1}$$

where $V_{C\max}$, $V_{C\min}$ and $V_{C\mathrm{avg}}$ are the maximum, minimum, and average values of the voltage across the storage capacitor C_s for a batch of pulses.

Usually, the charging does not involve predictive algorithms. This means that when the output voltage reaches the programmed value, the inverter is shut down. At this moment, the converter components, e.g., the leakage inductance of the HV transformer, store remnant energy E_rem that is commensurable with energy portions transferred to C_s every cycle. Then, the output overshoots because E_rem may flow wholly or partially to the storage capacitor. This is one of the main factors degrading PPR. In fact, it seems to be the only factor discussed in literature. It might seem that the repeatability can be estimated easily, assuming that all this energy can be transferred to C_s; then, R would be proportional to E_rem. More precisely, it can be given by the formula (see the Appendix)

$$R = \left(\sqrt{1 + \frac{E_\mathrm{rem}}{E_\mathrm{c}}} - 1\right) \cdot 100\% \tag{2}$$

where E_c is the energy stored in C_s. Application notes from ALE [10] and General Atomics [4], [11] provide similar simplistic estimates. In scientific experimentation, it is common to set the charge voltage at a fraction of the charger rated voltage and/or charge small capacitors. Then, the charge can be accomplished during even less than a half-cycle of the conversion frequency [see Figs. 7 and 15(a)], which means that E_rem is comparable with E_c. Assuming that $E_\mathrm{rem} = E_\mathrm{c}$, we calculate $R = 41.4\%$. If it takes two cycles to reach the maximum charge voltage, we can assume that $E_\mathrm{rem} = 0.25E_\mathrm{c}$, which yields

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TABLE I
MAIN SPECIFICATIONS

Input Voltage	400 VAC or $480VAC^{+10\%}_{-14\%}$, 3Φ 50/60 Hz, 4 wire, frequency ± 2%
Output Voltage	0 to 10 kV
Average Charging Rate	20 kJ/s
PRR	Single shot to 1 kHz
Efficiency	>92 % at full charging rate, >85 % at 30 % of rated power
Power factor	>0.93 at full charging rate >0.85 at 30 % of rated power
Pulse to Pulse repeatability	Better than 1% at 1 kHz@10 kV, long-term
	Better than 0.8% at 1 kHz@10 kV, short-term Better than 2% at 1 kHz@2 kV-10 kV, short-term.
Insulation	Air, 10 kV and below
Size	10½" (6U)H x 19"W x 24"D rack mount
Weight	90 lb (41 kg)
Cooling	Air

$R = 11.8\%$ (see Fig. 20); in reality, the repeatability may be not that bad.

Much effort was put to improve PPR, particularly at high PRR. A common approach is decreasing the rate of charge by an order of magnitude or so toward the end-of-charge (EOC). Thus, the charge buckets (using the terminology of [4], [10]) carried in each period are smaller, and the energy delivery to the storage capacitor can be controlled tighter. This technique in various implementations is used in commercial products (see, e.g., [3], [4], [12]). The shortcoming of such an approach is overrating the charger power, since the bulk high-power charge occurs at a low duty cycle, fine charging capturing 10–30% of the charge cycle [3].

This paper describes the development and testing of a high-power charger satisfying the aforementioned contradicting requirements within the constraints of a low-cost proven technology. A focus is made on the theoretical and experimental investigation of PPR. In this paper, the latter was studied at bulk charge only.

II. MAIN SPECIFICATIONS

This section summarizes in Table I the salient features and the most important technical parameters of the developed charger.

III. DESIGN

A charger block diagram is shown in Fig. 1. The charger is comprised of a 3-phase input rectifier with a circuit breaker, a soft-start means and a smoothing filter, a converter module (CM), and an HV divider and control means. Triggered by an external source, the charger charges capacitor C_s that is discharged onto a dummy load via a high-power switch DSw. Limiting inductors and/or resistors may be added as needed.

The CM is comprised of an inverter INV, an HV transformer wound on popular U100/57/25 ferrites, and a rectifier R. The CM's heart is a halfbridge quasi-resonant inverter

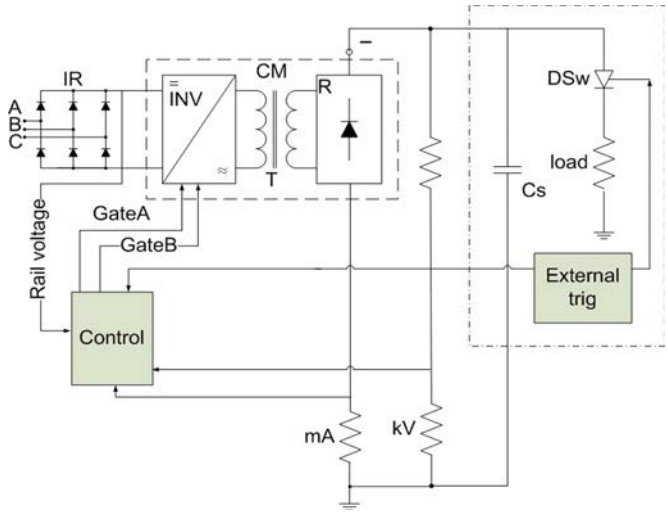

Fig. 1. Charger block diagram.

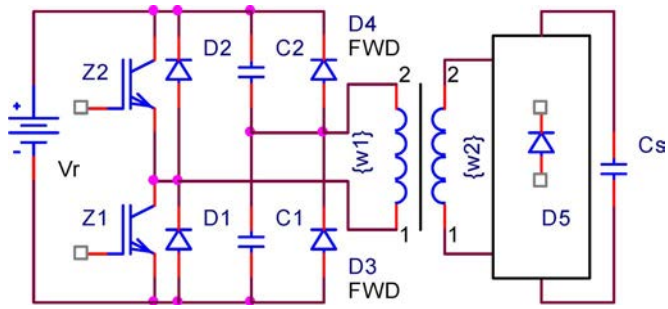

Fig. 2. Halfbridge inverter with energy dosing capacitors. Transformer is actually comprised of two transformers, whose primaries are connected in parallel and secondaries in series.

with energy-dosing capacitors (Fig. 2) [14]–[16]. Work [15] provides the principle and theory of operation (its content is partially reiterated, cleaned of misprints, and expanded in this section and in the Appendix). In normal mode, one of the resonant capacitors, C1, C2, is charged to the rail voltage V_r. When the corresponding switch closes, the resonant capacitor discharges through the primary winding, while its counterpart recharges to the rail voltage (see also timing diagrams Fig. 21). If the current path contains an inductance, a sine waveform is generated, and, ideally, all the energy stored in both resonant capacitors is transferred to the secondary side. If the resonant capacitor discharges fully but the current does not fall to zero, the freewheeling diode (FWD), which is connected in parallel to the capacitor, conducts, acting as a clamp and preventing voltage reversal. Thus, the remainder of the energy stored in the circuit inductance is transferred to the output. The benefits of the energy-dosing are tight control of the energy transfer and inherent limitation of the short-circuit current and voltages across the converter components.

The maximum frequency, at which the operation is possible at a certain load voltage V_l with zero-current crossing (ZCC), in a normalized form is given by [15]

$$f_N(V_l, E) = \frac{1}{\frac{2}{\pi}\left[\frac{1}{2}a\cos\left(\frac{V_l}{V_l - E}\right) + \frac{E}{2V_l}\sqrt{1 - \frac{2V_l}{E}}\right]} \quad (3)$$

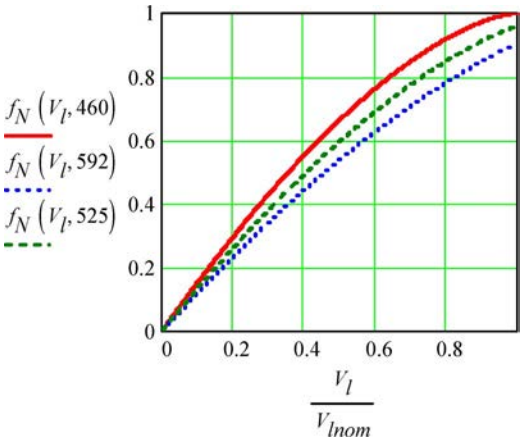

Fig. 3. ZCC curves for low (460 V), high (592 V), and nominal (525 V) dc rail voltages. $V_{\rm lnom}$ is nominal load voltage.

where E is the rail voltage, and both the rail and the load voltages are referenced to the same side of the transformer. The conversion frequency f is normalized to the resonant frequency f_0 of the loop formed by the leakage inductance and the resonant capacitors; $f_N = f/f_0$. A sample plot of this equation is shown in Fig. 3.

Since energy dosing is implemented, the charging power P is proportional to conversion frequency

$$P = 2C_{\rm r}V_{\rm r}^2 f$$

where $C_{\rm r}$ is the capacitance of the resonant capacitors C1 and C2. The load voltage can be calculated as [15]

$$V_l = 2E\sqrt{\frac{C_{\rm s}}{C_{\rm r}}ft}. \tag{4}$$

Although P cannot be expressed as an explicit function of time, the time to charge to a specified load voltage $t_{\rm ch}$ can be. Combining (3) and (4), we obtain in a normalized form

$$t_{\rm chN} = \frac{C_{\rm s}}{C_d}\frac{\pi V_l^2\left[1 - a\cos\left(\frac{V_l}{E-V_l}\right)\right] + EV_l\sqrt{\frac{E-2V_l}{E}}}{4\pi E^2} \tag{5}$$

where $t_{\rm chN} = t_{\rm ch}f_0$.

Using (5) and recognizing that the charging power $P = (d/dt)(C_{\rm s}V_l^2/2)$, we can plot the load voltage, charging power, and frequency versus time, as shown in Fig. 4, in a normalized form. It can be seen that the power is not increasing linearly as in the systems with constant current charge but rather saturating to EOC. There are two implications to this end: 1) the charge can be accomplished faster, at a price of some overloading of the converter components at start of charge (about 50% higher start currents, albeit at a lower frequency—Figs. 6 and 11); and 2) lower energy/charge bucket delivered to the storage capacitor at EOC, which is beneficial for PPR. A detailed comparison of the two charge methods is, however, beyond the scope of this paper.

The field-programmable-gate-array-based controls are characterized by their flexibility ensuing from programming and digital processing capabilities. The standard features include multiple protections (short circuit, overheat, overcurrent, and overvoltage, arc, etc.,) and means of voltage and current setting.

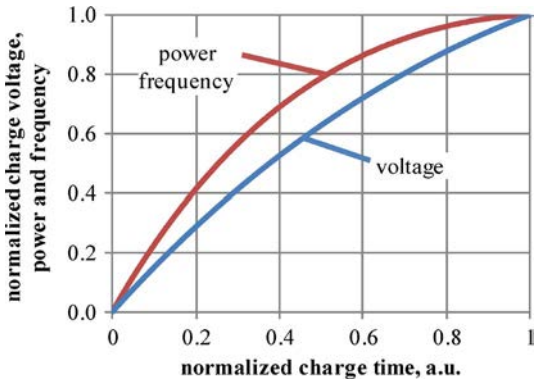

Fig. 4. Time dependence of load voltage, charging power, and frequency at ZCC.

Via a firmware, an algorithm realizing (3) is implemented. It adapts the switching frequency from 12.5–55 kHz, in such a way as to ensure zero-current switching (ZCS) for all possible scenarios, keeping maximum duty cycle for high power. Thus, the switching losses are virtually non-existent, which allows using relatively slow inexpensive semiconductor switches both on the primary and secondary sides.

A precision feedback divider was designed for high-fidelity measurements necessary for maintaining good PPR. A risetime of less than 1 μs and low temperature drift were realized.

The packaging was made in a $19''$ rack-mounted chassis, $10\ 1/2''$-tall, $24''$-deep. The parasitics of the HV transformer together with the capacitors C1, C2 are integrated into the resonant tank circuit, so no external chokes are needed. The circuit breaker and an HV connector are mounted on the rear panel. On the front view [Fig. 5(a)], the front panel borrowed from the Spellman SR6 series [17] is seen. The unit is equally divided by height into two sections. The upper half houses a conservatively designed input rectifier with the circuit breaker, EMI filters and soft start components, and the inverter. HV components, a housekeeping power supply, and the filtering electrolyte capacitors of the input rectifier are located in the bottom half [Fig. 5(b)]. The control board is mounted on the front panel. Owing to high efficiency (see Section V-C), all-air cooling is feasible.

Comprehensive PSpice models accounting for numerous parasitic parameters and mimicking controls for the frequency variation were developed, assisting in both the design and interpretation of the experimental data. A sample of the simulated waveforms is given in Fig. 6 for the cases of low and high line voltages. With the purpose of shortening the computation time and for clearer graphical presentation, in these simulations, $C_{\rm s}$ was 200 nF, approximately half of that used in the experiments. It is seen that, at any moment (except the first pulse that is chopped intentionally) during the charging cycle, ZCS is attained. This was confirmed experimentally (see Section V-B).

IV. Repeatability Analysis

Pulse-to-pulse *variability* evolves from several factors.

1) Converter remnant energy $E_{\rm rem}$ at EOC. $E_{\rm rem}$ may flow wholly or partially to the storage capacitor, so the output voltage will be higher than the programmed value.

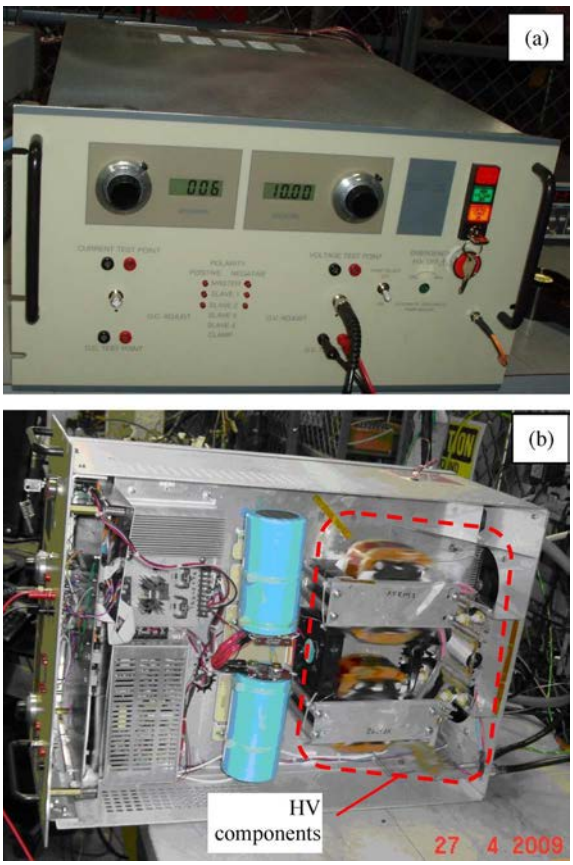

Fig. 5. Charger (a) front view and (b) bottom section.

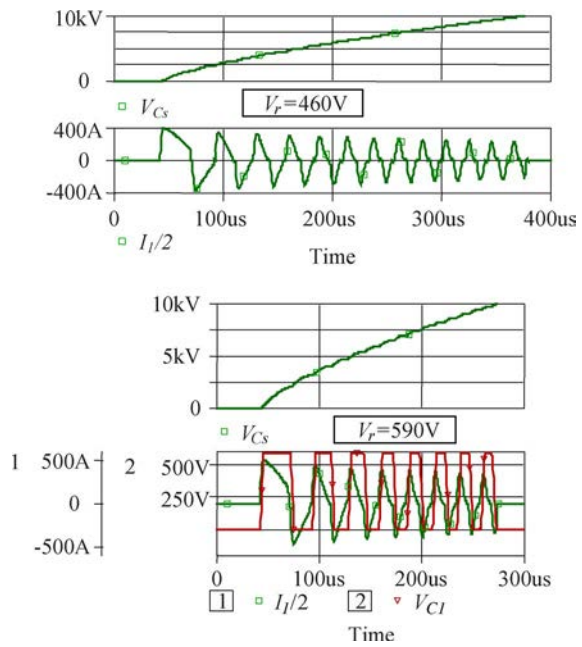

Fig. 6. PSpice simulation for 460 V and 590 V dc rail voltage. Parameters correspond to those of physical object (leakage inductance is L = 3.3 mH, reflected to secondary; C1 = C2 = 2 μF is resonant capacitor, $C_{\rm s} = 200$ nF is the storage capacitance). Primary current I_1 is halved.

2) Error in generating EOC signal. This may be caused by a poor-quality feedback, noise, unstable reference voltage, etc.

3) Delay t_d between the EOC and the actual insulated-gate bipolar transistor (IGBT) turn-off. It comprises digital delays, optocouplers delay, and the IGBT turn-off delay. Even constant t_d, if commensurable with half-period, affects PPR. Depending on the circuitry and the components, t_d can be fractions of a microsecond, i.e., t_d is a good part of the half-period.

The open literature cites factor 1 only as detrimental to PPR. However, factor 2 can be quite as important. A rule of thumb is that, in relatively low-voltage applications *and* low-noise environment, *and* charge intervals comprising just a few cycles of conversion frequency, factor 1 dominates. On the contrary, at high voltage in a noisy environment and long charge, factor 2 would dominate. In the present work, factor 2 accounts for roughly 60% of the pulse-to-pulse variability at the maximum charge voltage. Quantifying further the influence of the cited factors is beyond the scope and means of this paper.

It is logical to assume that $E_{\rm rem}$, on the average, is proportional to the rail voltage squared, and $E_{\rm rem}$ depends upon the value of the primary/secondary current at EOC. With our broad definition, $E_{\rm rem}$ can be stored anywhere in the system: in the leakage and magnetizing inductances and parasitic capacitance of the HV transformer and rectifier, in the parasitic inductances of the busbars and connections, etc. For the sake of simplicity, we disregard factors 2 and 3 and will limit the analysis to the case of $E_{\rm rem}$ stored in the leakage inductance only.

In the circuit in question, $E_{\rm rem}$ flows not only into $C_{\rm s}$, but is recovered partially in the dc rail power supply and, depending on the initial conditions (IC), may be directed to the resonant capacitors C1, C2; part of it is lost in the form of heat. Upon the transistor opening at EOC, if the corresponding resonant capacitor is not fully discharged (mode 1), with reference to Fig. 2, the transformer current flows along the following loops (we have chosen arbitrarily the bottom switch as the conducting one): positive terminal of C1, HV transformer, HV rectifier D5, $C_{\rm s}$, FWD D2, $V_{\rm r}$, returning to C1. The FWD current is split in two, half of it recharging one of the divider capacitors C2. If FWD parallel to C1 conducts at EOC (mode 2), the current loop does not include C1, but closes through D3. There also can be a transition from mode 1 to mode 2.

Sample PSpice waveforms for a low charge voltage of 2 kV (the charger is rated for 10 kV) are shown in Fig. 7; they will be useful as an empirical guide for further analytical analysis. In this parametric run, the source of the variability was the dc rail voltage $V_{\rm r}$, swept from 460–600 V in 20-V increments, which corresponds to common variations of a 400 VAC 3-phase line. EOC corresponds to the chopping of the primary winding current I_1.

It is seen that the maximum overshoot takes place not at the maximum chopping current. Moreover, the same chopping current (same amount of energy stored in $L_{\rm s}$) may result in very different overshoots depending on the EOC timing, as follows from the comparison of the first and the last curves ($V_{\rm r} = 460$ V, $V_{\rm r} = 600$ V, respectively). Calculating by (2), the overshoot ΔV above the programmed voltage of 2 kV, which would result from $E_{\rm rem}$ delivered wholly to $C_{\rm s}$, we obtain $\Delta {\rm V} \approx 450$ V. In this example, $E_{\rm rem} = L_{\rm s} I_2^2/2 = 0.2$ J for $I_1 = 500$A corresponding to $V_{\rm r} = 460$ V, $V_{\rm r} = 600$ V. It

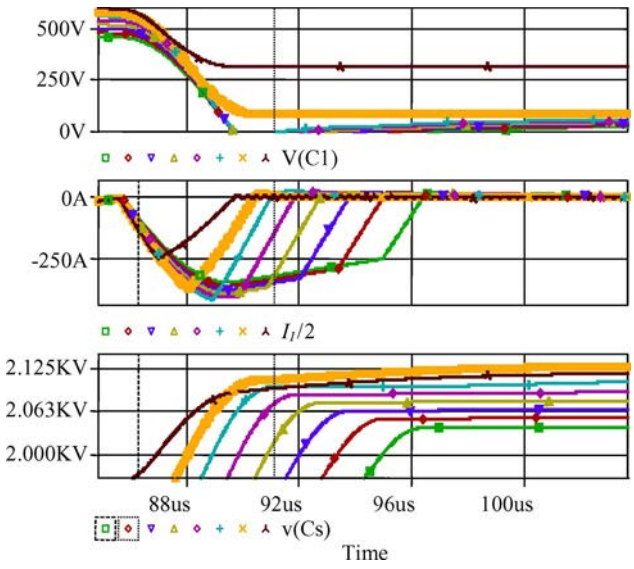

Fig. 7. Programmed charge voltage 2 kV. $V_{\rm r} = 460$ V, 480 V, ..., 600 V. $C_{\rm s} = 200$ nF. Primary current I_1 is halved. Curves corresponding to largest overshoot are in thicker lines.

is seen that the overvoltages are much lower than the above estimates even at higher currents. Thus, only part of $E_{\rm rem}$ reaches $C_{\rm s}$, the rest being recuperated mainly in the dc rail source. An additional observation is that the largest overshoot (lower graph Fig. 7, 2nd curve from the left) occurs when the resonant capacitor voltage does not reach zero.

Linearizing the circuit piecewise and using corresponding equivalent circuits (EC) allows full analytical description of the electromagnetic processes occurring after EOC; IC can be obtained from the equations derived in [15].

An analytical treatment is given in the Appendix. In this paper, it is limited to a worst case of EOC occurring at any time from the primary current onset to its maximum. Full rigorous analysis and a predictive control algorithm derived from it will be reported separately. For the converter parameters corresponding to our experimental setup and simulations[1], the repeatability R, is plotted in Fig. 8 versus EOC time $t_{\rm c}$ (subscript "c" stands for *C*hopping). The load voltage V_L serves as a parameter and is given as a fraction of the rail voltage; both V_L and $V_{\rm r}$ reflected to the same side of the HV transformer. Since a halfbridge is involved, the nominal load voltage is $V_L \approx V_{\rm r}/2$ at *low* line. Considering $V_{\rm r}$ variation from 460 V (low line) to 590 V (high line), we note that the repeatability is worse at high line, whereas the nominal load voltage is $V_L = 10$ kV $\approx V_{\rm r}/2 * 460/590 * k_{tr} = 0.39 k_{tr} V_{\rm r}$. The maxima of the curves indicate the worst case of the most unfavorable EOC timing and are plotted separately in Fig. 9 together with a plot of (2). It is seen that the overshoot derived empirically is by several times larger than that predicted by the rigorous analysis. Finally, Fig. 10 summarizes PSpice and analytical calculations and experimental results. The latter are described in more detail in Section V-D. Notably, the analytical curve lies very close to its PSpice counterpart, always above it, as it should, because the

[1]200 nF in simulations, 400 nF in experiments.

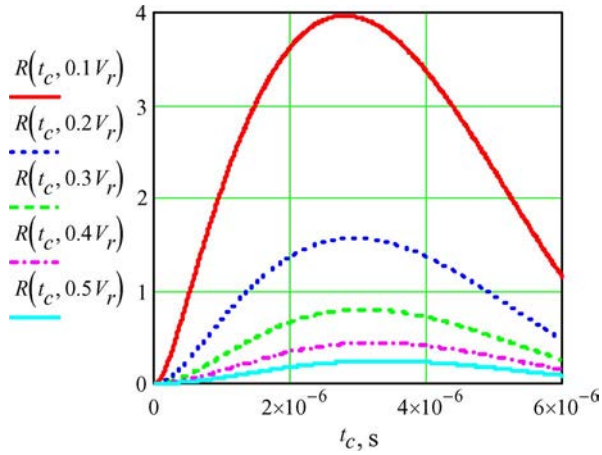

Fig. 8. Repeatability R % versus $t_{\rm c}$, with load voltage V_L as a parameter (in fractions of the rail voltage, both reflected to the same side of HV transformer). Nominal load voltage (10 kV) is $V_L \approx V_{\rm r}/2$ for low line ($V_{\rm r} = 460$ V at primary side). $C_{\rm s} = 200$ nF, C1 = C2 = 2 μF. Compare to Fig. 7.

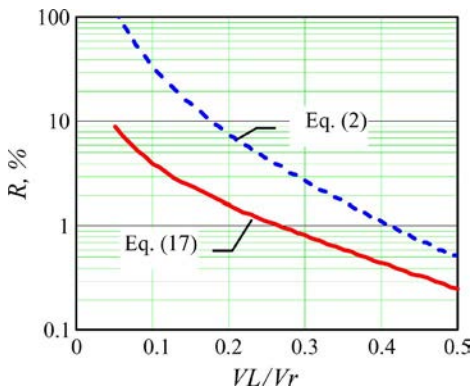

Fig. 9. Repeatability as a function of charge voltage, $C_{\rm s} = 200$ nF, C1 = C2 = 2 μF, worst case.

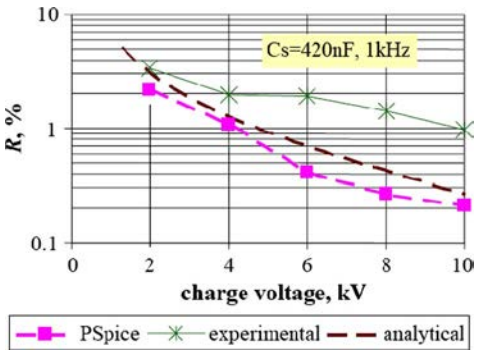

Fig. 10. Repeatability as a function of charge voltage—summary of PSpice and analytical calculations and experimental results.

PSpice parametric sweeps performed in 20-V $V_{\rm r}$ increments do not necessarily find precisely the worst-case EOC time.

V. Experimental

A. Measurement Means

For the measurement of the high-frequency current of the inverter components, Rogowski probes of PEM make, model CWT15, were used. The $C_{\rm s}$ voltage was measured by a

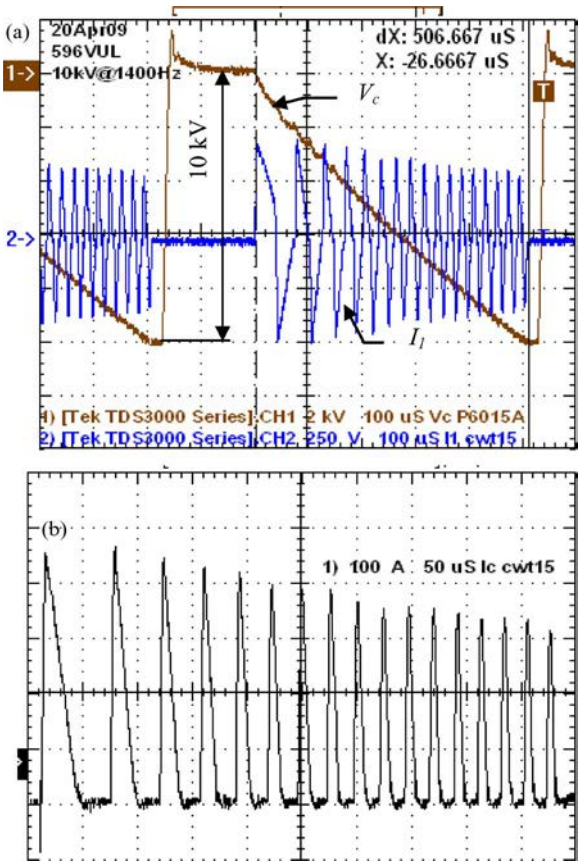

Fig. 11. Typical waveforms at high line. PRR = 1400 Hz in burst, charge time is 507 μs. (a) Load capacitor voltage and primary winding current. (b) Collector current.

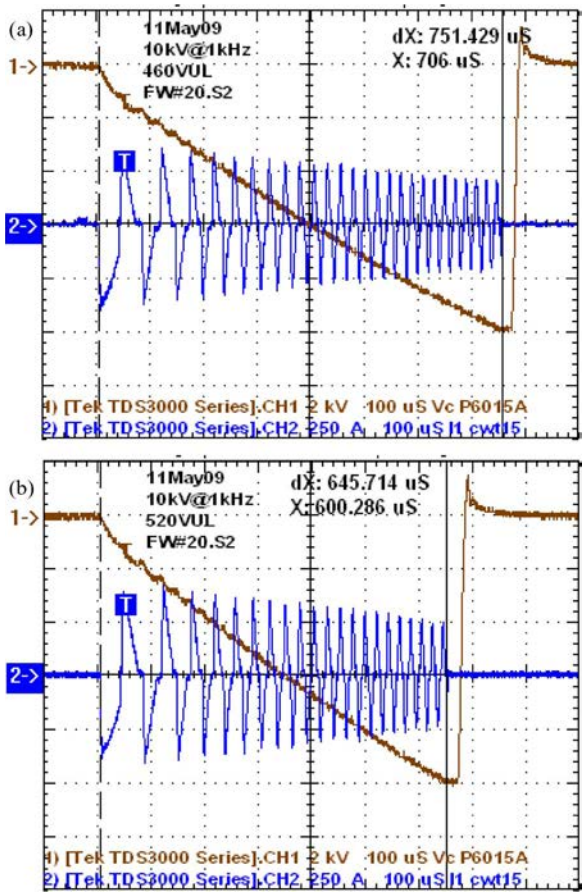

Fig. 12. Typical waveforms at 10 kV at 1000 Hz at (a) low and (b) nominal line.

Tektronix P6015A probe. Floating voltage measurements were performed by a differential Tektronix probe P5200. Efficiency and power factor were measured with a Voltech power meter, model PM300. Temperatures were monitored by thermocouples connected to an Agilent data logger, model 34970A, with supporting BenchLink software.

B. Waveforms

One of the main goals of this work was realizing the highest efficiency possible by enforcing lossless switching in all possible scenarios at all charge levels and repetition rates. The noise immunity of the control circuitry in this sense is also an important issue. A thorough experimental investigation, side by side with PSpice modeling, was performed. We found that, under no circumstances, ZCS was disturbed. Several figures below illustrate the results. Fig. 11(a) shows $V_{\rm c}$ and primary winding current I_1 in burst operation at a PRR of 1400 Hz for $C_{\rm s} = 420$ nF (charge rate of 29.4 kJ/s), with the collector current $I_{\rm c}$ of one of the transistors displayed on expanded scale in Fig. 11(b). The information on horizontal and vertical scales per division here and in further plots is indicated in the waveforms' annotations.

Note that the experimental $V_{\rm c}$ curves appear to be closer to a linear function than their theoretical counterpart Fig. 4. This discrepancy results from generous deadtime absent in the analytical treatment.

At low line (longest charge), $C_{\rm s} = 420$ nF is charged in 750 μs [Fig. 12(a)], so continuous operation with such load is limited to a PRR of 1 kHz, if ample deadtime is desirable between the shots. At higher line voltage, the charge is accomplished faster [Figs. 11(a) and 12(b)]. As clearly seen in Fig. 11(b), the conversion frequency adapts to keep high duty cycle yet maintaining ZCS. The highest conversion frequency is 55 kHz at low line, with a very large margin guaranteeing ZCS without any shoot-through currents even at abnormal line sags.

C. Efficiency and Power Factor

The efficiency is calculated from the values of the input and load power, the former being measured by a Voltech PM300 power meter. Measuring the load power is indirect. It is actually calculated as the energy per shot delivered to the storage capacitor $(\mathrm{E} = C_{\rm s} \cdot V_{\rm c}^2/2)$ multiplied by PRR. At full power, the efficiency was about 92%, and power factor was 94% (Fig. 13). The efficiency values are lower by 1–2% than expected and what could be deducted from the loss measurement (see [18] for methods of the IGBT loss measurement), and intuitively from the amount of the dissipated heat. We note that the IGBTs' baseplate overheat was less than 40 °C at all operational modes. One of the possible sources of error is a low-accuracy $V_{\rm c}$ measurement (the probe P6015A is specified at $\pm$3% dc attenuation, excluding the oscilloscope error; we minimized this error

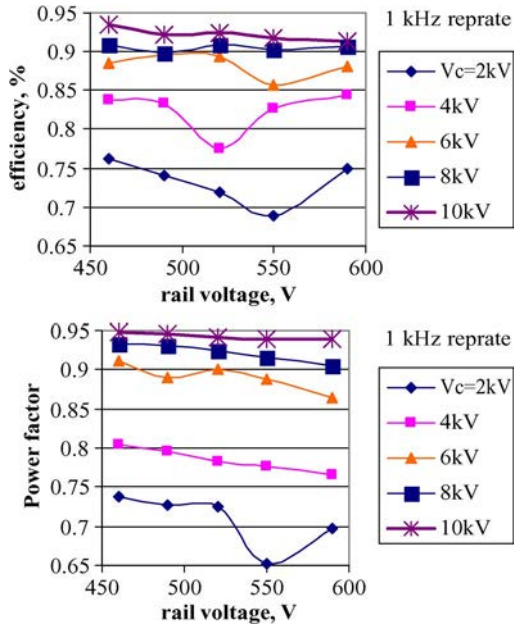

Fig. 13. Efficiency and power factor dependence on rail voltage for several charge voltages.

by careful calibration). Every percent of voltage measurement error is translated to 2% of the energy measurement error, so the uncertainty of the efficiency measurement is quite pronounced.

D. Repeatability

We will distinguish here between short-term and long-term PPR. The former is defined as that derived from N*consecutive* pulses. In our measurements, $\mathrm{N} = 80$, sampled from the 121st to the 200th pulse. Thus, the short-term PPR is not influenced by thermal drifts, aging of components, etc. It is affected by the rail voltage variations to the extent of the high-frequency rail voltage ringing, excluding slow input changes. Long-term PPR is also influenced by the rail voltage variation in the full specified range, for instance, from 460 to 590 VDC (corresponding to $400VAC^{-10\%}_{-14\%}$). In this paper, the reference to long-term PPR is made in the light of such variations, other parameters being not controlled.

PPR measurements were taken using the FastFrame capability of a DPO7054 scope. Up to four signals were monitored simultaneously. The load voltage V_{c} was measured again by the P6015A probe, but on a 100-mV scale with a 10-V offset allowing the signal at EOC fit the screen. In addition, the feedback voltage V_{fdbk} (with the same sensitivity and offset) and primary current were monitored. The shortcoming of these *direct* measurements is their low resolution, of the order of several bits of the scope vertical resolution. Arguably, a better technique is differential measurement, e.g., monitoring the difference between the feedback voltage and the programming voltage. In such a way, at EOC, the scope would see virtually zero voltage. In the differential measurement, the feedback voltage was biased with a voltage equal to the programming value. After finding fair matching of the V_{c} and differential V_{fdbk} data, we continued with direct V_{c} measurement only.

The scope was triggered by the EOC event. In these experiments, the discharge switch DSw was fired 20 μs after EOC.

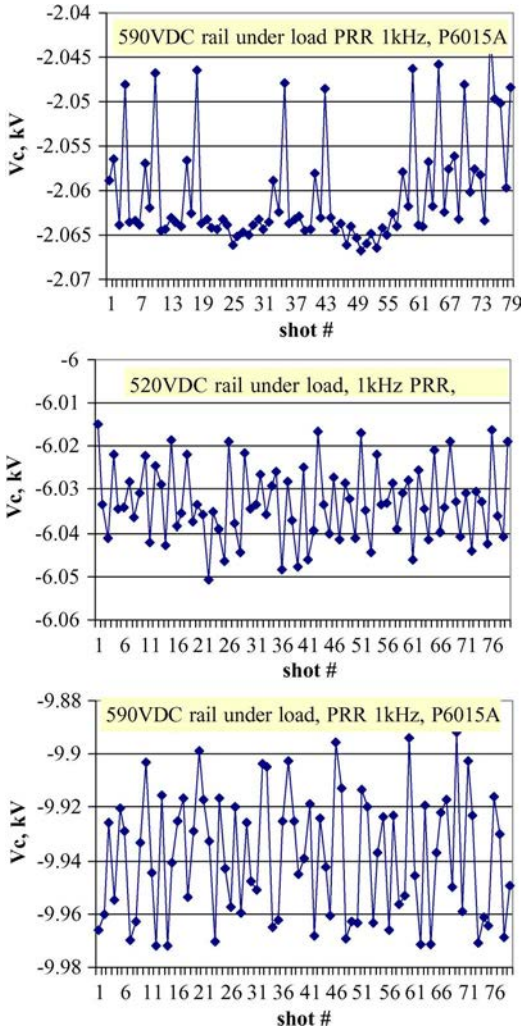

Fig. 14. Shot-to-shot variability taken with FastFrame. $C_{\mathrm{s}} = 420$ nF, 1 kHz reprate, 2-kV, 6-kV, and 10-kV settings. See inset annotations for rail voltage.

The first 800 shots were collected with a 500-point resolution on a 4-μs/div scale. The waveforms were saved as screen captures, and 80 frames, starting from the 121st frame, were saved in the csv format. An Excel spreadsheet was designed, in which 79 shots[2] were processed; they are graphed in Fig. 14 for several rail voltages showing V_{c} pulse-to-pulse variation.

Three typical screenshots of the overlays of 80 frames are shown in Fig. 15. They correspond to the data of Fig. 14 and show where the variability, at least partially, evolves. At EOC, the primary current is chopped at random. If there is a certain pattern (as seen at 2-kV and 6-kV settings), PPR is better. When the current is chopped at an arbitrary time point (10-kV setting), at the rising and trailing edges and at zero, PPR deteriorates. It still remains below 1% at the maximum voltage and PRR, owing to specifics of the used converter topology and high conversion frequency.

For three rail voltage settings, namely 460, 520, and 590 VDC, PPR was calculated by the formula that looks in an

[2]Values shown are averages of 50 points, starting from 250 pnt of the acquisition (approximately the middle part of the screen Fig. 15).

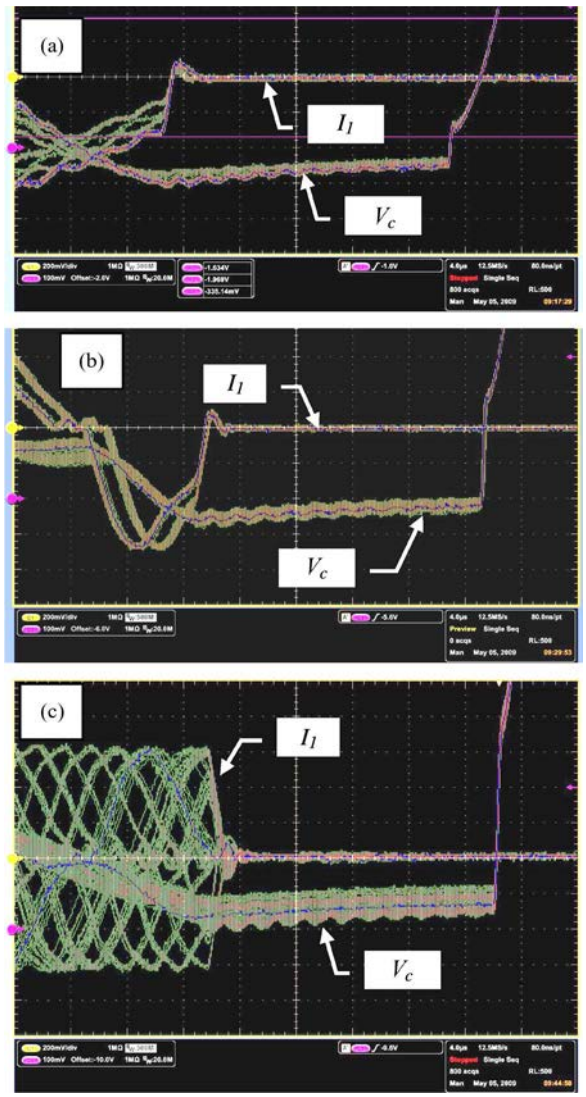

Fig. 15. Overlay of 80 frames (V_c—100 V/div, I_1—100 A/div) for: (a) high line, 2 kV at 1 kHz; (b) nominal line, 6 kV at 1 kHz; and (c) high line, 10 kV at 1 kHz. Horizontal 4 μs/div.

Excel convention as follows:

$$R = \frac{\min(A2:C80) - \max(A2:C80)}{average(A2:C80)} * 100 \qquad (6)$$

where columns A-C contain each V_c values for 79 consecutive pulses, for 460, 520 and 590 VDC, respectively, i.e., $3 \times 79 = 237$ pulses. Alternatively, we varied the line voltage continuously from the low to high level, looking for the least stable operation, i.e., for the largest V_c variation. For this method, PPR was calculated by (1) using $V_{C\max}$, $V_{C\min}$ values from the whole measurement range.

The short- and long-term PPR are plotted in Figs. 16 and 17, respectively. The experimental curves shown in Fig. 17 are calculated by (1), (6); they are labeled as "*overall experimental*", and "*3 rail experimental*", respectively. Thus, every point of the first curve is built from many thousands shots, and every point of the second one comprises 237 shots. The variability is larger than that predicted by the theory accounting for factor 1 only

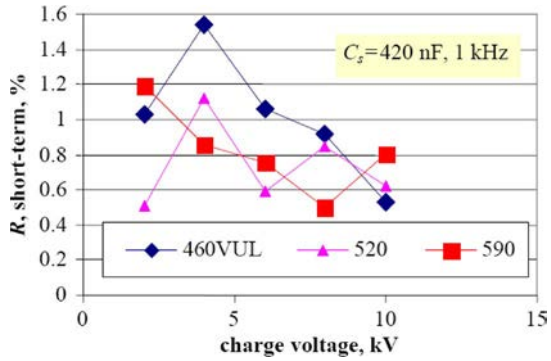

Fig. 16. Short-term repeatability.

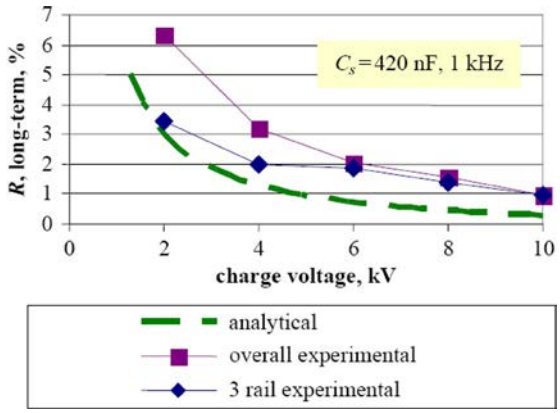

Fig. 17. Long-term repeatability as a function of charge voltage—summary of analytical calculations and experimental results.

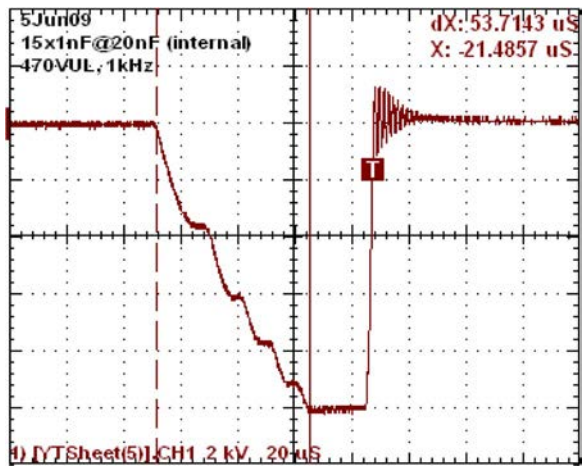

Fig. 18. 33-nF capacitor assembly under test. Charge time is 53 μs.

("analytical" curve). This discrepancy can be attributed to the measurement errors and propagation delays (factors 2, 3).

All the above results pertain to the experiments with $C_s = 420$ nF. Additional measurements were taken with much smaller $C_s = 33$ nF. A typical charge waveform is shown in Fig. 18. Short charge time allows much higher PRR, up to 7 kHz, leaving ample time between the charge cycles. However, with our SCR-based discharge switch, we cannot operate the system at such high PRR.

Remarkably, although the current chopping at EOC occurs at random (Fig. 19), even with this very low capacitance, PPR

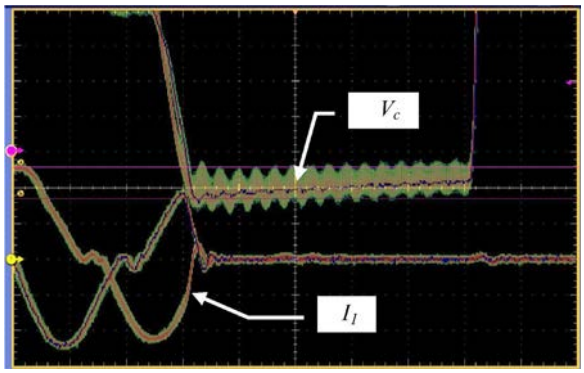

Fig. 19. Overlay of 600 frames (Vc—100 V/div, I1–200 A/div) $C_s = 33$ nF; 10 kV at 1 kHz, $V_r = 470$ VUL. Horizontal 4 μs/div.

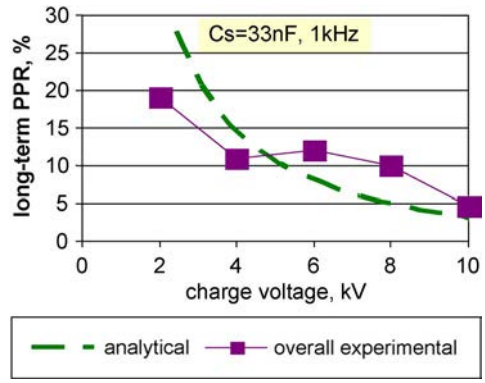

Fig. 20. PPR at low-capacitance charge.

is better than 1% at 10 kV and Vr = 470 V. However, with continuous V_r variation, PPR is worse. A summary of the results is shown in Fig. 20. We note that the analytical curve is not valid if the charge occurs during one two half-cycles, which is the case for the 2-kV and 4-kV voltage setting.

At the time of writing this paper, the charger was in continuous operation for 3000 hrs, having generated more than 10^{10} 10-kV shots at 1 kHz, with the test ongoing.

VI. Conclusion

This development has been a test case for low-cost generic technology of high repetition rate high-voltage high-power highly efficient capacitor charging. A crossover of 10-kV, 20-kJ/s, and 1-kHz PRR specifications was chosen for the demonstration. An energy-dosing converter topology with smart controls optimizing the switching frequency for high efficiency was used. The switching is accomplished at a frequency of up to 55 kHz employing relatively slow inexpensive IGBTs. High efficiency allowed a compact all-air cooled design. Good PPR was demonstrated.

A rigorous repeatability analysis has been performed, as far as we know, for the first time in open literature. The obtained results allow accurate evaluation of achievable long term PPR for energy-dosing resonant topologies. They also can be extended to the case of classic series resonant converters. Improving the measurements can narrow the gap between the theoretical limit, as put forth by the analytical treatment, and the experimental results, for the long-term repeatability. In addition, the derived

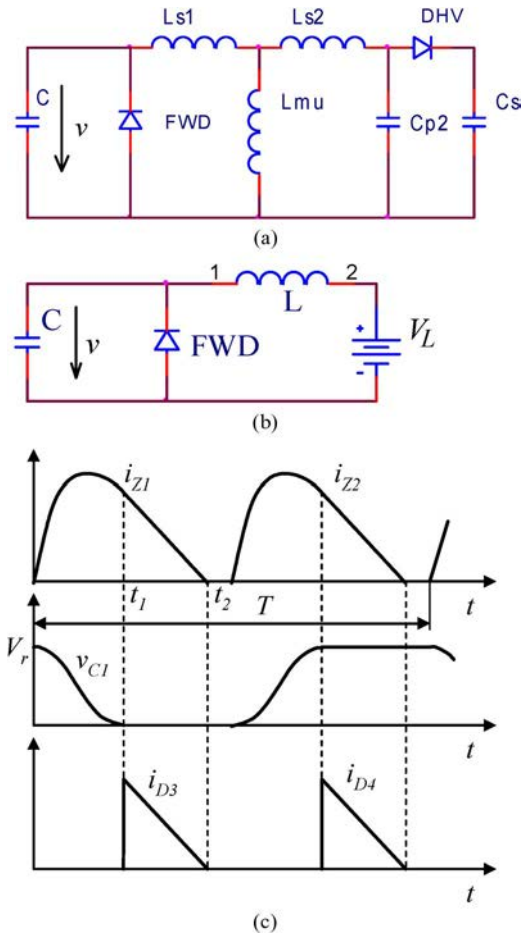

Fig. 21. (a) Full equivalent circuit. (b) Reduced equivalent circuit. (c) Timing diagrams in normal operation (see Fig. 2 for notation).

equations have allowed building a predictive control algorithm, thus paving the road for a dramatic PPR improvement without any slowing of the charge rate. This work will be reported later. Only worst-case analysis is presented in full in this paper.

Appendix

The EOC signal is generated when the charge voltage reaches a preset value. This can occur at any time within the transistor conduction interval, and even during the deadtime, since some residual energy $E_{\rm rem}$ still circulates in the system. If the programmed load voltage is calculated as $V_L = \sqrt{2E_{\rm c}/C_{\rm s}}$, and the real charge voltage is $V_L + \Delta V_L = \sqrt{2(E_{\rm c} + E_{\rm rem})/C_{\rm s}}$, assuming that $E_{\rm rem}$ is delivered to $C_{\rm s}$, we transform (1) to a form

$$R = \sqrt{1 + \frac{E_{\rm rem}}{E_{\rm c}}} - 1. \tag{7}$$

Equation (7) is a simplistic PPR assessment giving largely overstated values (see Introduction).

The last half-period preceeding EOC starts as usual, with one of the resonant capacitors charged to the rail voltage, and the other fully discharged. We neglect here the rail/busbar voltage oscillations and the FWD forward drop. A full-scale EC is shown in Fig. 21(a). Here, $C = 2{\rm C}1 = 2{\rm C}2$, diode

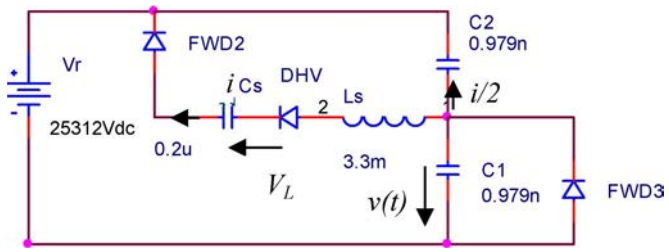

Fig. 22. Equivalent circuit after EOC. FWD2 is parallel to transistor, DHV stands for HV rectifier. All parameters are reflected to secondary. Ls current is split equally between Vr and C2 if FWD3 does not conduct.

DHV denotes the HV rectifier. A T-equivalent circuit of the transformer is used, where Ls1, Ls2 are the leakage inductances of the primary and the secondary windings, respectively, Lmu is the magnetizing inductance, Cp2 is the transformer parasitic capacitance. *All parameters and variables are reflected to the secondary*.

Full circuit is too complicated for analytical treatment. In our case of the transformer with a closed magnetic system, the magnetizing current can be neglected. Likewise, in high-power applications, the parasitic capacitances of the HV transformer and rectifier can be neglected. We assume also that the load voltage $V_L \equiv V_C$ does not change much during a half-period of the conversion frequency; hence, the storage capacitor can be represented by a counter electromotive force equal to the load voltage. This common assumption works well if the charge is accomplished in two or more periods of the conversion frequency. Then, the circuit Fig. 21(a) reduces to that of Fig. 21(b), and the correspondent equations and timing diagrams can be borrowed from [15]. Here, L is the transformer leakage inductance.

The inductance L current and the resonant capacitance C voltage before t_1 are given as (a misprint made in [15] is corrected)

$$i_1 = \frac{V_\mathrm{r} - V_L}{\rho}\sin\omega t, \quad v_1 = (V_\mathrm{r} - V_L)\cos\omega t + V_L \tag{8}$$

where $\omega = 1/\sqrt{LC}$, $\rho = \sqrt{L/C}$.

After EOC has been generated at time t_c, the EC transforms to that of Fig. 22. The values are for reference only. This EC is valid until the clamping FWD starts conducting. With the current and voltage directions as indicated by the arrows, the circuit is described by the differential equation

$$\frac{d^2v}{dt^2} + \omega^2 v = \omega^2(V_L + V_\mathrm{r}). \tag{9}$$

Equation (8) provides IC for the analysis

$$i_1(t_\mathrm{c}) = \frac{V_\mathrm{r} - V_L}{\rho}\sin(\omega t_\mathrm{c})$$

$$v_1(t_\mathrm{c}) = (V_\mathrm{r} - V_L)\cos(\omega t_\mathrm{c}) + V_L \tag{10}$$

or, restarting from zero the time count for the EC Fig. 22

$$i_1(0) = \frac{V_\mathrm{r} - V_L}{\rho}\sin(\omega t_\mathrm{c}), \quad \frac{dv_1}{dt}(0) = -\frac{i(0)}{C}. \tag{11}$$

Equation (9) with IC (10) has a solution

$$v = (V_L - V_\mathrm{r})\sin\omega t_\mathrm{c}\cdot\sin\omega t + [(V_\mathrm{r} - V_L)\cos\omega t_\mathrm{c} - V_\mathrm{r}]\cos\omega t + V_\mathrm{r} + V_L \tag{12}$$

wherefrom the inductor current is

$$i = \frac{1}{\rho}\left[(V_\mathrm{r} - V_L)\sin\omega(t + t_\mathrm{c}) - V_\mathrm{r}\sin\omega t\right]. \tag{13}$$

It crosses zero at a time point T_ei

$$T_{ei} = \frac{1}{\omega}arctg\frac{(V_L - V_\mathrm{r})\sin\omega t_\mathrm{c}}{(V_\mathrm{r} - V_L)\cos\omega t_\mathrm{c} - V_\mathrm{r}}. \tag{14}$$

Depending upon the EOC time C_s and the load voltage, the latter increases after EOC by

$$\Delta V_L = \frac{1}{C_\mathrm{s}}\int_0^{T_{ei}} i dt. \tag{15}$$

There is some inconsistency in this analysis, because the clamping action of the FWD is not accounted for. A more correct approach would be to check if and where voltage v reaches zero, integrate to the time of the voltage crossing zero, and continue the analysis from this point using a simpler equivalent circuit that is a subset of Fig. 22, with C1, C2 out of action. However, we simplify the analysis at this point, assuming that in the worst-case scenarios, C does not discharge fully. This assumption is borne by formal analysis, simulations and experiment.

After some derivations, we obtain the output overshoot

$$\Delta V = \frac{C}{C_\mathrm{s}}\left\{(V_\mathrm{r} - V_L)\left[\cos\omega t_\mathrm{c} - \cos(\omega T_{ei} + \omega t_\mathrm{c})\right] - V_\mathrm{r}(1 - \cos\omega T_{ei})\right\} \tag{16}$$

and the repeatability R % as defined by (1), ($V_{Cavg} = V_L$, in a closed form

$$R = \frac{100}{V_L}\frac{C}{C_\mathrm{s}}\left\{(V_\mathrm{r} - V_L)\left[\cos\omega t_\mathrm{c} - \cos(\omega T_{ei} + \omega t_\mathrm{c})\right] - V_\mathrm{r}(1 - \cos\omega T_{ei})\right\}. \tag{17}$$

Equations (12)–(17) are valid if v does not reach zero before i does.

Introducing a nondimensional variable $v_l = V_L/V_\mathrm{r}$, we rewrite (17) as

$$R = 100\frac{C}{C_\mathrm{s}}\left\{(1/v_l - 1)\left[\cos\omega t_\mathrm{c} - \cos(\omega T_{ei} + \omega t_\mathrm{c})\right] - 1/v_l(1 - \cos\omega T_{ei})\right\} \tag{18}$$

which is plotted in Fig. 23; (16) is plotted in Fig. 24 for $V_\mathrm{r} = 550$ V. In these calculations, C1 = C2 = 2 μF (C = 1.958 nF), $C_\mathrm{s} = 200$ nF. It is seen that the maximum error occurs at a t_c that is slightly smaller than a quarter of the period of the resonant frequency $T = \omega/2\pi$.

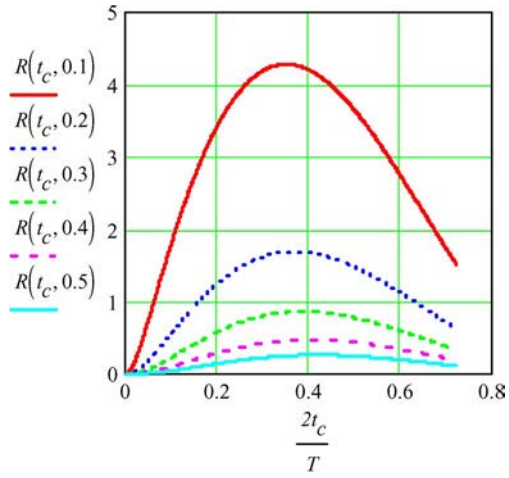

Fig. 23. Repeatability R % versus chopping point t_c, with normalized load voltage v_l as a parameter. $T = 2\pi/\omega$.

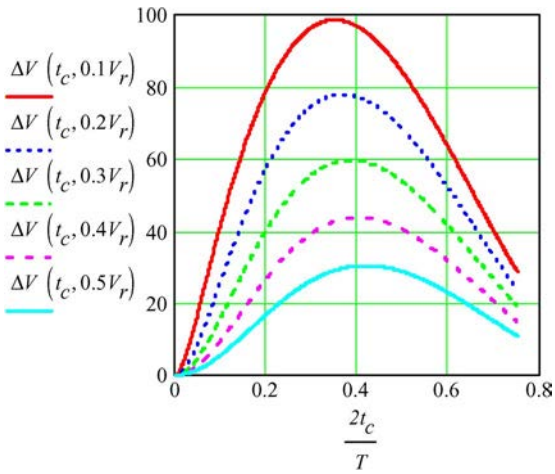

Fig. 24. Load voltage overshoot dependence on EOC timing t_c for $V_r = 550$ V. Load voltage in fractions of V_r serves as parameter.

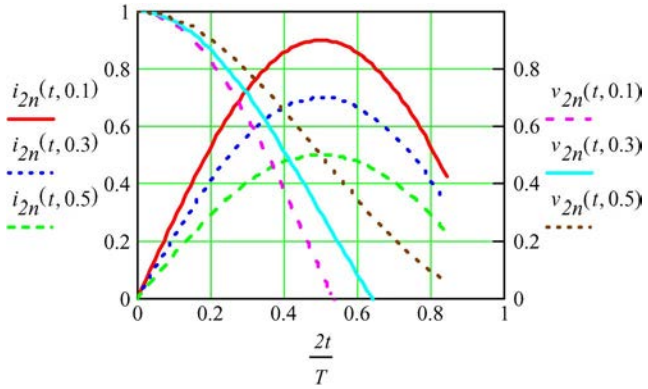

Fig. 25. Normalized inductor current and resonant cap voltage. v_l serves as a parameter.

Looking again at (8) and rewriting them in a normalized form

$$i_{2n} = (1 - v_l)\sin\omega t, \quad v_{2n} = (1 - v_l)\cos\omega t + v_l \tag{19}$$

where $i_{2n} = i_2/I_0$, $I_0 = V_r/\rho$, $v_{2n} = v_2/V_r$, we note that the resonant capacitors do not discharge to zero before $t_c \sim 0.5T$, which is shown in Fig. 25.

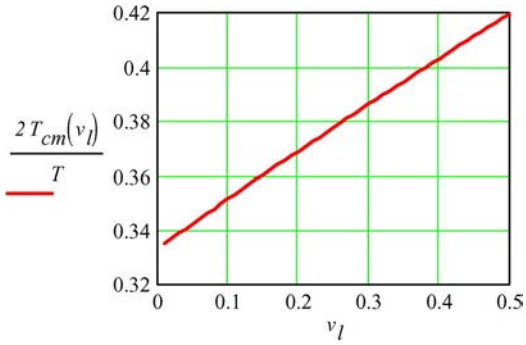

Fig. 26. Worst chopping moment versus normalized load voltage.

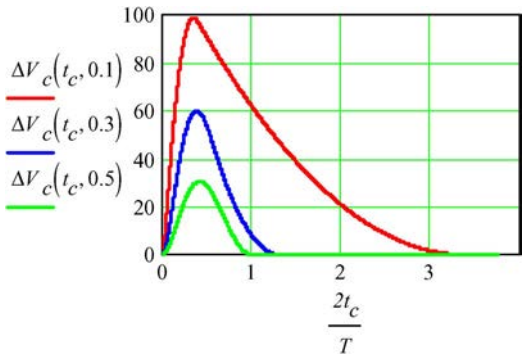

Fig. 27. Load voltage increment dependence on EOC timing t_c for $V_r = 550$ V. Compare to Fig. 24.

Alternatively, we can solve

$$\frac{dR(t_c, V_l)}{dt_c} = 0 \tag{20}$$

for t_c, thus finding at what t_c R reaches maximum. This time point is designated as T_{cm}. The expressions are too bulky to reproduce here, but the solution plotted in Fig. 26, in conformity with Fig. 25, clearly indicates that the worst PPR corresponds to the EOC time point, at which the resonant capacitors do not discharge fully. A rigorous analysis involving sequential ECs is even more complex; we give an example chart Fig. 27 corroborating the validity of the aforementioned statements. Thus, the worst-case analysis is complete.

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Costel Carp (M'07), photograph and biography not available at the time of publication.

Clifford Scapellati (M'92), photograph and biography not available at the time of publication.